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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/510,375	02/22/00	WILLIAMS B	303.164US3

021186 TM02/0925
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EXAMINER	
KIM, H	
ART UNIT	**PAPER NUMBER**
2185	

DATE MAILED: 09/25/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/510,375	Williams
Examiner	**Group Art Unit**
H. Kim	2185

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Response

A SHORTENED STATUTORY PERIOD FOR RESPONSE IS SET TO EXPIRE 3 (three) MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a response be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for response is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication .
- Failure to respond within the set or extended period for response will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☒ Responsive to communication(s) filed on 6/25/01, CPA.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 26-39 is/are pending in the application.

Of the above claim(s)_____ is/are withdrawn from consideration.

☐ Claim(s)_____ is/are allowed.

☒ Claim(s) 26-39 is/are rejected.

☐ Claim(s)_____ is/are objected to.

☐ Claim(s)_____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The proposed drawing correction, filed on_____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on_____ is/are objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 11 9(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number)_____.

☐ received in this national stage application from the International Bureau (PCT Rule 1 7.2(a)).

*Certified copies not received:_____.

Attachment(s)

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 9

☐ Interview Summary, PTO-413

☐ Notice of References Cited, PTO-892

☐ Notice of Informal Patent Application, PTO-152

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Other_____

Office Action Summary

Detailed Action

Continued Prosecution Application

1. The request filed on 6/25/01 for a Continued Prosecution Application (CPA) under 37 CFR 1.53(d) based on parent Application No. 09510375 is acceptable and a CPA has been established. An action on the CPA follows.

2. Claims 26-39 are presented for examination. This office action is in response to the amendment filed on 6/25/01.

3. Receipt is acknowledged of information disclosure statement filed on 6/25/01, which the statement has been placed of record in the file. Information disclosed and listed on PTO 1449 was considered.

4. Applicants are request to summit a priority correction statement to change the priority date.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

6. Claims 26, 29, 32 and, 35-39 are rejected under 35 U.S.C. 102(a) as being anticipated by "Intel" Electronic News, (EN) December 5, 1994 in view of 82430FX PCIset DATASHEET 82437FX System CONTROLLER (TSC) AND 82438FX DATA PATH UNIT (TDP), Intel Corp., pp 1-67, 11/96 (INTEL).

As to claims 26, 29, 32 and, 35-39, *EN* discloses the invention as claimed. *EN* discloses Triton PCI Chip set. It is inherent that a computer system comprising a processor, a bus, a memory system, a memory controller including the first and second memory devices are page mode memory and the Burst EDO memory respectively. These inherent features are disclosed by Intel (Fig. 1 and pp 1, 24, 31, and 41-45).

See MPEP 2124 and 2131.01 for multiple reference 35 U.S.C. 102 rejections.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 27-28, 30-31, 33, and 34 are rejected under 35 U.S.C. 103(a) as being anticipated by "Intel" Electronic News, (EN) December 5, 1994 in view of 82430FX PCIset DATASHEET 82437FX System CONTROLLER (TSC) AND 82438FX DATA PATH UNIT (TDP), Intel

Corp., pp 1-67, 11/96 (INTEL) and further in view of Fung et al. (Fung) US Patent No. 5,630,163.

As to claims 27-28, 30-31, 33, and 34, *EN and Intel* disclose the invention substantially as claimed in the above claim. Although Intel discloses that DRAM types are determined by BIOS (which implies that DRAM types are determined during a power up sequence and system includes a power up detection circuit to start a BIOS sequence), however, neither En nor Intel specifically discloses a power supply; and a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller; wherein the processor is responsive to at least information from the memory to program the memory controller to provide the first set of access control signals to the memory at a first time and the second set of access control signals to the memory at a second time.

Fung disclose a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller (col. 1 lines 25-32, BIOS read on this limitation since the BIOS operates during a power up routine) for the purpose of determining a computer configuration thereby guaranteeing reliable operation of the system. Also it would have been readily appreciated by one of ordinary skill in the art that a system includes a power supply to provide a power to the system.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the

invention was made to include the power supply and a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller of Fung into the combined invention of EN and Intel for the advantages stated above.

9. Claims 26, 29, 32 and, 35-39 are rejected under 35 U.S.C. 103(a) as being anticipated by Farrer et al. (Farrer) US Patent No. 5,307,320 in view of Micron, "Reduce DRAM cycle times with extended data-out", Micron technical Note pp 5-33 thru 5-40, 4/94 and further in view of Wyland US Patent No. 5,261,064.

As to claims 26, 29, 32 and 35-39 *Farrer* discloses a system, comprising:

a bus (Fig. 1 Ref. 105) for transferring information;

a memory (Fig. 1 Ref. 103), coupled to the bus, comprised of a memory device which is interchangeably of a mode selected from the group consisting of a first mode (Fig. 3 Ref. 301) and a second mode (Fig. 3 Ref. 302), the memory having a first set of access control signal timing requirements for the first mode and a second set of access control signal timing requirements for the second mode;

a programmable memory controller (col. 5 lines 16 and 54-66), coupled to the bus and to the memory, capable of providing the first set of access control signal timing requirements and the second set of access control signal timing requirements to the memory; and

a processor (Fig. 1 Ref. 101), coupled to the bus and the memory controller, responsive to at least information from the memory to program the memory controller to provide a set of access control signals to the memory in accordance with the memory device mode, wherein the information from the memory includes data read from the memory device.

However Farrer does not specifically disclose a memory, coupled to the bus, comprised of a memory device which is interchangeably of a mode selected from the group consisting of extended data out mode and fast page mode, the memory having a first set of access control signal timing requirements for the extended data out mode and a second set of access control signal timing requirements for the fast page mode.

Micron discloses a memory, coupled to the bus, comprised of a memory device which is interchangeably of a mode selected from the group consisting of extended data out mode and fast page mode, the memory having a first set of access control signal timing requirements for the extended data out mode and a second set of access control signal timing requirements for the fast page mode (page 5-33 bottom of right column and page 5-39 bottom of right column) thereby the user may base the design of the computer system on the type of memory that offers the target price/performance ration of the system. *Micron* further discloses that the memory device is interchangeable (page 5-33 bottom of right column and page 5-39 bottom of right column). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include the memory, coupled to the bus, comprised of a memory device which is interchangeably of a mode selected from the group consisting of extended data out

mode and fast page mode, the memory having a first set of access control signal timing requirements for the extended data out mode and a second set of access control signal timing requirements for the fast page mode of Micron in the invention of Farrer for the advantages stated above.

Furthermore neither Farrer nor Micron discloses a burst mode.
However it is well known in the memory art a memory can be operate in a burst mode. For example Wyland discloses burst mode of operation (abstract lines 2-3) in order to increase access time (col. 1 lines 15-16).
Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use burst access memory of Wyland in the combined invention of Farrer and Wyland for the purpose of increasing access time thereby increasing overall system performance.

10. Claims 27-28, 30-31, 33, and 34 are rejected under 35 U.S.C. 103(a) as being anticipated by Farrer et al. (Farrer) US Patent No. 5,307,320 Micron Reduce DRAM cycle times with extended data-out, Micron technical Note pp 5-33 thru 5-40, 4/94 and Wyland US Patent No. 5,261,064 and further in view of Fung et al. (Fung) US Patent No. 5,630,163.

As to claims 27-28, 30-31, 33, and 34, *Farrer, Micron, and Wyland* disclose the invention substantially as claimed in the above claim. However, neither Farrer, Micron, nor Wyland specifically discloses a power supply; and a power up detection circuit coupled to the processor

and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller; wherein the processor is responsive to at least information from the memory to program the memory controller to provide the first set of access control signals to the memory at a first time and the second set of access control signals to the memory at a second time.

Fung disclose a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller (col. 1 lines 25-32, BIOS read on this limitation since the BIOS operates during a power up routine) for the purpose of determining a computer configuration thereby guaranteeing reliable operation of the system. Also it would have been readily appreciated by one of ordinary skill in the art that a system includes a power supply to provide a power to the system.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include the power supply and a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller of Fung into the combined invention of Farrer, Micron, and Wyland for the advantages stated above.

Response to Amendment

11. Applicant's arguments filed on 6/25/01 have been fully considered but they are not persuasive.

Applicant's remarks on pages 2-6, the Examiner require to provide rational or evidence tending to show such inherency is not considered persuasive.
These inherent features are disclosed by Intel publication (11/96 (INTEL)). See MPEP 2124 for later publication showing factual evidence and 2131.01 for multiple reference 35 U.S.C. 102 rejections.

Applicant's remarks on pages 2-6, the references not showing a burst mode is not considered persuasive. Intel discloses a burst mode (page 1).

Also in response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, even though applicant's modification results in great improvement and utility over the prior art, it may still not be patentable if the modification was within the capabilities of one skilled in the art. In re Sola, 22 C.C.P.A. (Patents) 1313, 77 F.2d 627, 25 USPQ 433 ; In re Normann et al., 32 C.C.P.A. (Patents) 1248, 150 F.2d 708, 66 USPQ 308 ; In re Irmscher, 32 C.C.P.A. (Patents) 1259, 150 F.2d 705, 66 USPQ 314.

Those skilled in memory art must be presumed to know something about memory mode apart from what references disclose; it is immaterial that reference does not disclose specific function set forth in applicant's specification, since this is merely a different variation which would be obvious to one skilled in the art in a use which one skilled in the art, following teachings of prior art, might make of it. In re JACOBY, 135 USPQ 317 (CCPA 1962).

Therefore, the rejections are proper.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

13. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

14. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. § 1.111(c).

15. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

16. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Hong Kim whose telephone number is (703) 305-3835. The Examiner can normally be reached on the weekdays from 8:30 AM to 5:00 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Do Yoo, can be reached on (703) 308-4908.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

17. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 308-6296 or (703) 308-6165

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

HK
Patent Examiner
September 22, 2001